Claims

What is claimed is:

1. An integrated circuit, comprising:

a first circuit section formed in a substrate;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer formed under at least a portion of the first circuit section; and

a conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer, the conductive layer reducing an effective lateral resistance of the isolation buried layer, whereby an electrical isolation between the first and second circuit sections is increased.

2. The integrated circuit of claim 1, further comprising:

a plurality of conductive plugs formed in the substrate, the plugs providing a substantially low resistance path for electrically connecting the conductive layer to the isolation buried layer.

3. The integrated circuit of claim 1, wherein the conductive layer comprises:

a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

4. The integrated circuit of claim 3, wherein the net includes a plurality of holes therein, at least a portion of the first circuit section being formed in one or more holes in the net.

5. The integrated circuit of claim 3, wherein the net overlays at least a portion of the first circuit section.

6. The integrated circuit of claim 1, wherein the isolation buried layer is connected to a ground or reference source.

7. The integrated circuit of claim 1, wherein the conductive layer is formed at least in part of metal.

8. The integrated circuit of claim 1, further comprising:

a second isolation buried layer formed under at least a portion of the second circuit section; and

a second conductive layer formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer, the second conductive layer reducing an effective lateral resistance of the second isolation buried layer.

9. The integrated circuit of claim 8, further comprising:

a plurality of conductive plugs formed in the substrate, the plugs providing a substantially low resistance path for electrically connecting the second conductive layer to the second isolation buried layer.

10. The integrated circuit of claim 8, wherein the second conductive layer comprises:

a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a second net.

11. The integrated circuit of claim 10, wherein the second net includes a plurality of holes therein, wherein at least a portion of the second circuit section is formed in one or more holes in the second net.

12. The integrated circuit of claim 10, wherein the second net overlays at least a portion of the second circuit section.

13. The integrated circuit of claim 8, wherein the first and second conductive layers are electrically connected to separate ground or reference sources.

14. The integrated circuit of claim 8, wherein:

the second circuit section comprises at least one bipolar transistor device, the bipolar transistor device including a collector buried layer formed in the substrate above the second isolation buried layer.

15. The integrated circuit of claim 1, wherein:

the integrated circuit is a mixed signal integrated circuit;

the first circuit section comprises a digital circuit section; and

the second circuit section comprises an analog circuit section.

16. The integrated circuit of claim 1, wherein the isolation buried layer has a lower resistivity than the substrate.

17. The integrated circuit of claim 1, wherein the isolation buried layer is formed in the substrate at depth in a range from about 2 micrometers (μm) to about 5 μm from an upper surface of the substrate.

18. A method of fabricating a mixed signal integrated circuit device, the method comprising the steps of:

forming a first circuit section in a substrate;

forming a second circuit section in the substrate, the second circuit section being spaced laterally from the first circuit section;

forming an isolation buried layer in the substrate under at least a portion of the first circuit section;

forming a conductive layer on a surface of the integrated circuit, the conductive layer overlaying at least a portion of the first circuit section; and

forming a plurality of conductive plugs in the substrate for operatively electrically connecting the isolation buried layer to the conductive layer, whereby an effective lateral resistance of the isolation buried layer is reduced.

19. The method of claim 18, wherein the step of forming the conductive layer comprises:

forming a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

20. The method of claim 19, wherein:

the net includes a plurality of holes therein; and

at least a portion of the first circuit section is formed in one or more holes in the net.

21. The method of claim 18, further comprising the step of:

electrically connecting the conductive layer to a ground or reference source, whereby signals coupled to at least one of the conductive layer and the isolation buried layer are shunted to ground or to the reference source.

22. The method of claim 18, wherein:

the isolation buried layer is formed in the substrate at depth in a range from about 2 micrometers (μm) to about 5 μm from an upper surface of the substrate.

23. The method of claim 18, further comprising the step of:

forming a second isolation buried layer under at least a portion of the second circuit section;

forming a second conductive layer on a surface of the integrated circuit; and

forming a plurality of conductive plugs in the substrate for electrically connecting the second isolation buried layer to the second conductive layer, whereby an effective lateral resistance of the second isolation buried layer is reduced.

24. The method of claim 23, wherein the step of forming the second conductive layer comprises:

forming a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a second net.

25. The method of claim 24, wherein:

the second net includes a plurality of holes therein; and

at least a portion of the second circuit section is formed in one or more holes in the second net.

26. A semiconductor device formed on a semiconductor wafer, comprising:

a first circuit section formed in a substrate of the semiconductor wafer;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer formed under at least a portion of the first circuit section; and

a conductive layer formed on a surface of the semiconductor wafer and electrically coupled to the isolation buried layer, the conductive layer reducing an effective lateral resistance of the isolation buried layer, whereby an electrical isolation between the first and second circuit sections is increased.

27. The semiconductor device of claim 26, further comprising:

a plurality of conductive plugs formed in the substrate, the plugs providing a substantially low resistance path for electrically connecting the conductive layer to the isolation buried layer.

28. The semiconductor device of claim 26, further comprising:

a second isolation buried layer formed under at least a portion of the second circuit section; and

a second conductive layer formed on a surface of the semiconductor wafer and electrically coupled to the second isolation buried layer, the second conductive layer reducing an effective lateral resistance of the second isolation buried layer.

29. The semiconductor device of claim 28, further comprising:

a plurality of conductive plugs formed in the substrate, the plugs providing a substantially low resistance path for electrically connecting the second conductive layer to the second isolation buried layer.